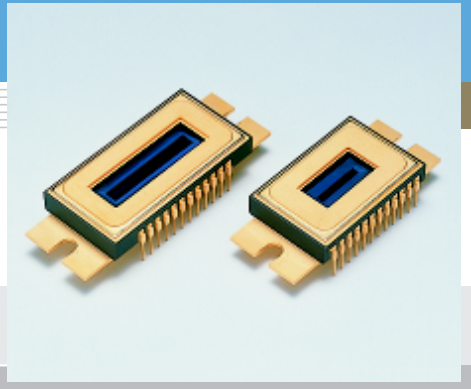


CCD area image sensor S7030/S7031 series

Back-thinned FFT-CCD



S7030/S7031 series is a family of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, S7030/S7031 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S7030/S7031 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S7030/S7031 series also features low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.

S7030/S7031 series has an effective pixel size of $24 \times 24 \mu\text{m}$ and is available in image areas ranging from $12.288 \text{ (H)} \times 1.392 \text{ (V)} \text{ mm}^2$ (512×58 pixels) up to a large image area of $24.576 \text{ (H)} \times 6.000 \text{ (V)} \text{ mm}^2$ (1024×250 pixels).

Features

- Non-cooled type: S7030 series
One-stage TE-cooled type: S7031 series
- Pixel size: $24 \times 24 \mu\text{m}$
- Line, pixel binning
- Greater than 90 % quantum efficiency at peak sensitivity wavelength
- Wide spectral response range
- Low readout noise
- Wide dynamic range
- MPP operation
- High UV sensitivity with good stability

Applications

- Fluorescence spectrometer, ICP
- Raman spectrometer
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm(H) × mm(V)]	Suitable multichannel detector head
S7030-0906	Non-cooled	532 × 64	512 × 58	12.288 × 1.392	C7040
S7030-0907		532 × 128	512 × 122	12.288 × 2.928	
S7030-0908		532 × 256	512 × 250	12.288 × 6.000	
S7030-1006		1044 × 64	1024 × 58	24.576 × 1.392	
S7030-1007		1044 × 128	1024 × 122	24.576 × 2.928	
S7030-1008		1044 × 256	1024 × 250	24.576 × 6.000	
S7031-0906	One-stage TE-cooled	532 × 64	512 × 58	12.288 × 1.392	C7041
S7031-0907		532 × 128	512 × 122	12.288 × 2.928	
S7031-0908		532 × 256	512 × 250	12.288 × 6.000	
S7031-1006		1044 × 64	1024 × 58	24.576 × 1.392	
S7031-1007		1044 × 128	1024 × 122	24.576 × 2.928	
S7031-1008		1044 × 256	1024 × 250	24.576 × 6.000	

General ratings

Parameter	Specification
Pixel size	24 (H) × 24 (V) μm
Vertical clock phase	2 phases
Horizontal clock phase	2 phases
Output circuit	One-stage MOSFET source follower
Package	24 pin ceramic DIP (refer to dimensional outlines)
Window	Quartz glass *1

*1: Window-less and AR-coated sapphire glass are available upon request.

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	Visv	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-10	-	+15	V
IGH voltage	VIG1H, VIG2H	-10	-	+15	V
SG voltage	VSG	-10	-	+15	V
OG voltage	VOG	-10	-	+15	V
RG voltage	VRG	-10	-	+15	V
TG voltage	VTG	-10	-	+15	V
Vertical clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	18	20	22	V	
Reset drain voltage	VRD	11.5	12	12.5	V	
Output gate voltage	VOG	1	3	5	V	
Substrate voltage	VSS	-	0	-	V	
Test point (vertical input source)	Visv	-	VRD	-	V	
Test point (horizontal input source)	VISH	-	VRD	-	V	
Test point (vertical input gate)	VIG1V, VIG2V	-8	0	-	V	
Test point (horizontal input gate)	VIG1H, VIG2H	-8	0	-	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH	4	6	8	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	4	6	8	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	4	6	8	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	4	6	8	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	4	6	8	V
	Low	VTGL	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	MHz
Vertical shift register capacitance *2	CP1V, CP2V	-	3,000	-	pF
Horizontal shift register capacitance *2	CP1H, CP2H	-	120	-	pF
Summing gate capacitance	CSG	-	7	-	pF
Reset gate capacitance	CRG	-	7	-	pF
Transfer gate capacitance	CTG	-	120	-	pF
Charge transfer efficiency *3	CTE	0.99995	0.99999	-	-
DC output level *4	Vout	12	15	18	V
Output impedance *4	Zo	-	3	-	kΩ
Power consumption *4 *5	P	-	15	-	mW

*2: S7030/S7031-1007

*3: Charge transfer efficiency per pixel, measured at half of the full well capacity.

*4: The values depend on the load resistance. (Typical, VOD=20 V, Load resistance=22 kΩ)

*5: Power consumption of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Saturation output voltage	Vsat	-	Fw × Sv	-	V	
Full well capacity	Vertical	150,000	300,000	-	e ⁻	
	Horizontal	300,000	600,000	-		
CCD node sensitivity	Sv	1.8	2.2	-	μV/e ⁻	
Dark current *6	DS	-	25 °C	4,000	12,000	e ⁻ /pixel/ s
MPP mode (tentative data)			0 °C	200	600	
Readout noise *7	Nr	-	8	16	e ⁻ rms	
Dynamic range *8	Line binning	18,750	75,000	-	-	
	Area scanning	9,375	37,500	-	-	
Photo response non-uniformity *9	PRNU	-	±3	±10	%	
Spectral response range	λ	-	200 to 1100	-	nm	

*6: Dark current nearly doubles for every 5 to 7°C increase in temperature.

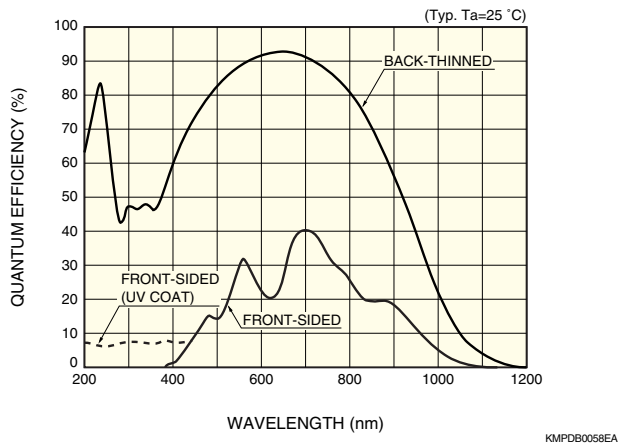
*7: Operating frequency is 150 kHz.

*8: Dynamic range (DR) = Full well/Readout noise

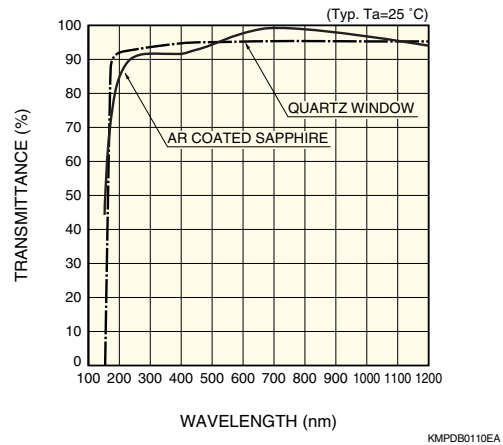
*9: Measured at the half of the full well capacity output.

$$\text{Photo response non-uniformity (PRNU) [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

■ Spectral response (without window) *10



■ Spectral transmittance characteristics



*10: Spectral response with quartz glass (or AR-coated sapphire glass) is decreased by the transmittance

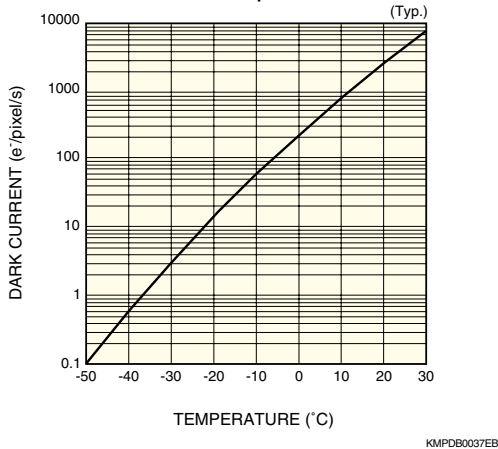
● Window material

Type No.	Window material
S7030/S7031 series	Quartz glass *11 (option: window-less, AR-coated sapphire glass *12)
S7032 series (two-stage TE-cooled types)	AR-coated sapphire glass *12 (option: window-less)

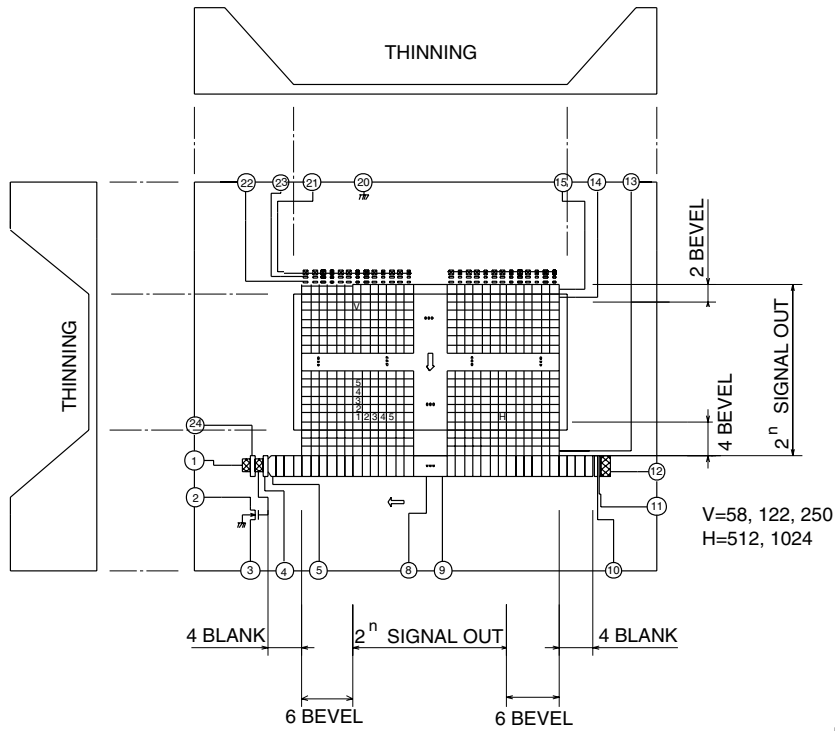
*11: Resin sealing

*12: Hermetic sealing

■ Dark current vs. temperature

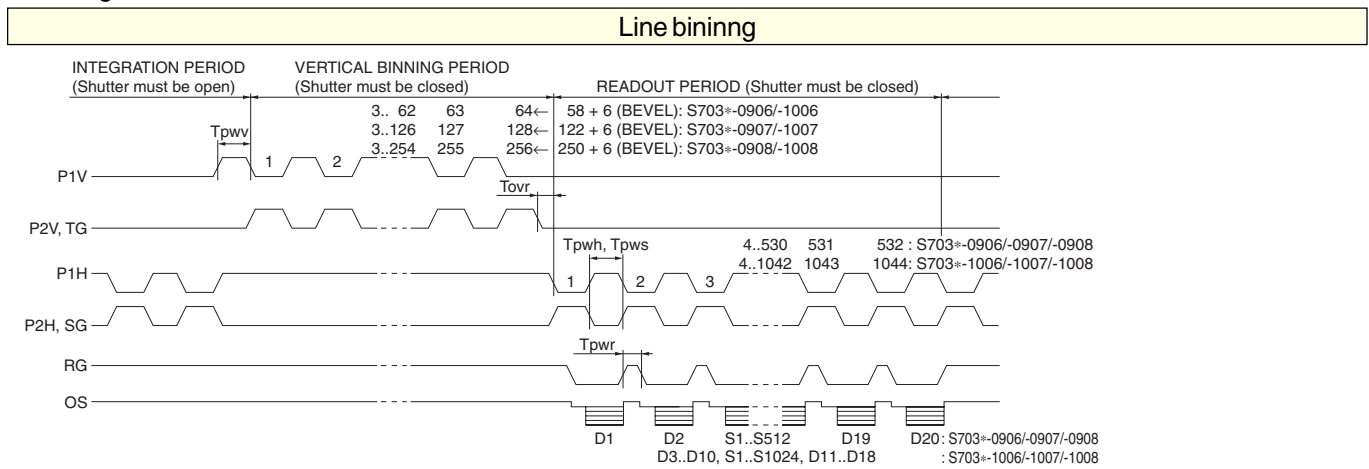


■ Device structure



KMPDC0016EB

■ Timing chart



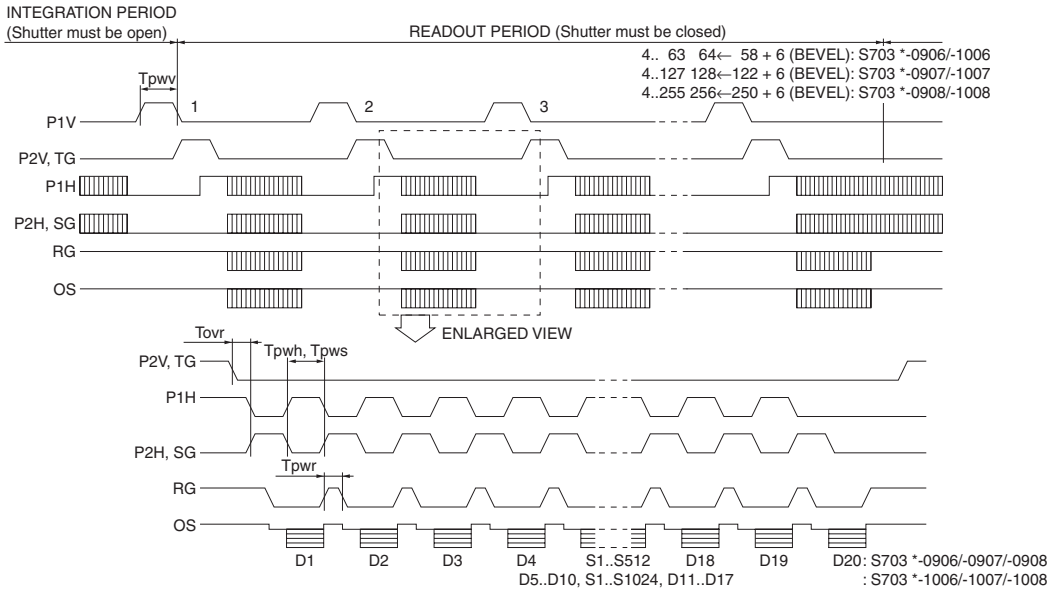
KMPDC0017EB

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	T_{pwv}	*13	6 *14	-	-	μ s
	Rise and fall time	T_{prv}, T_{pfv}		200	-	-	ns
P1H, P2H	Pulse width	T_{pwh}	*13	500	-	-	ns
	Rise and fall time	T_{prh}, T_{pfh}		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	T_{pws}	-	500	-	-	ns
	Rise and fall time	T_{prs}, T_{pfs}		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	T_{pwr}	-	100	-	-	ns
	Rise and fall time	T_{prr}, T_{pfr}		5	-	-	ns
TG - P1H	Overlap time	T_{ovr}	-	3	-	-	μ s

*13: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

*14: In case of S7030/S7031-0908, -1007.

Area scanning 1: low dark current mode



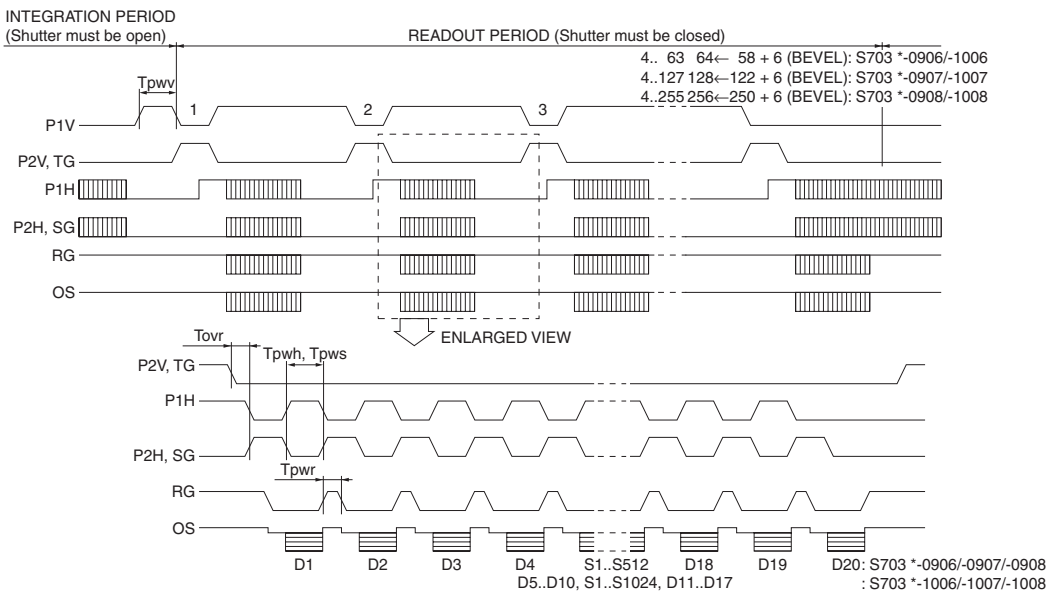
KMPDC0126EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpww	*16	6 *17	-	-	μs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*16	500	-	-	ns
	Rise and fall time	Tprh, pfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfhs	-	10	-	-	ns
	Duty ratio	-	-	-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tprf	-	5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	μs

*16: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

*17: In case of S7030/S7031-0908, -1007.

Area scanning 2: large full well mode



KMPDC0127EA

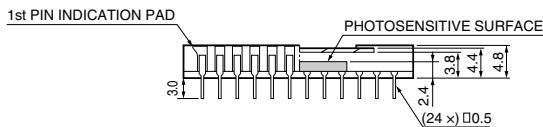
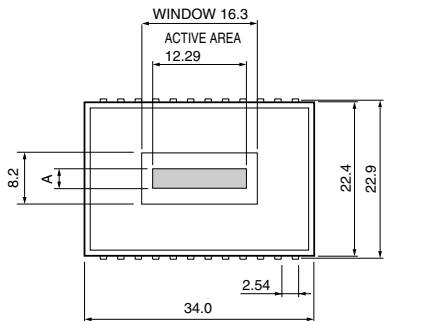
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	T_{pww}	*18	6 *19	-	-	μs
	Rise and fall time	T_{prv}, T_{pfv}		200	-	-	ns
P1H, P2H	Pulse width	T_{pwh}	*18	500	-	-	ns
	Rise and fall time	T_{prh}, T_{pfh}		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	T_{pws}	-	500	-	-	ns
	Rise and fall time	T_{prs}, T_{pfs}		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	T_{pwr}	-	100	-	-	ns
	Rise and fall time	T_{prr}, T_{pfr}		5	-	-	ns
TG - P1H	Overlap time	T_{ovr}	-	3	-	-	μs

*18: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

*19: In case of S7030/S7031-0908, -1007.

■ Dimensional outlines (unit: mm)

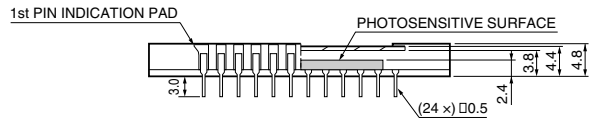
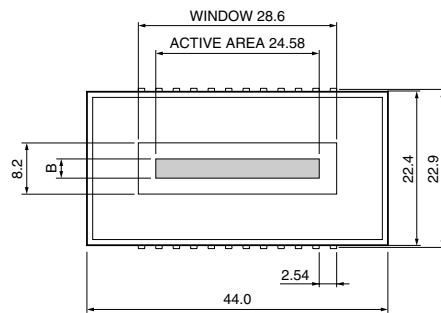
S7030-0906/-0907/-0908



S7030-0906: A=1.392
S7030-0907: A=2.928
S7030-0908: A=6.000

KMPDA0048EC

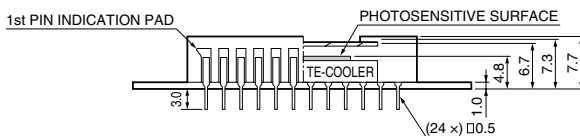
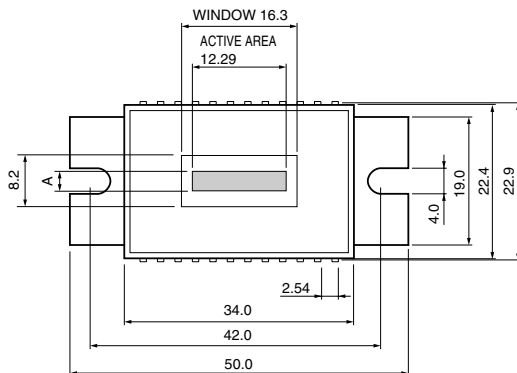
S7030-1006/-1007/-1008



S7030-1006: B=1.392
S7030-1007: B=2.928
S7030-1008: B=6.000

KMPDA0047EC

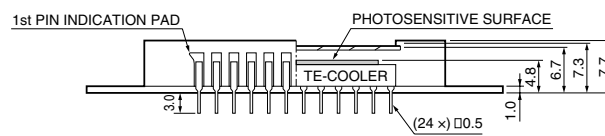
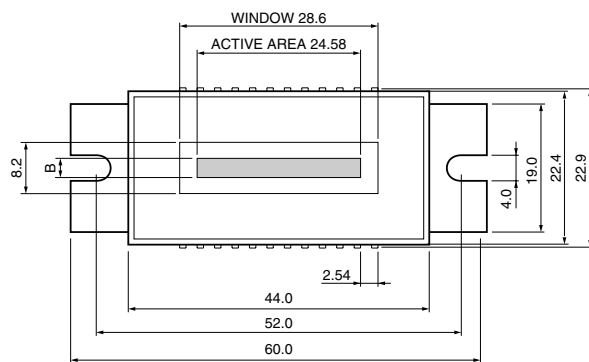
S7031-0906/-0907/-0908



S7031-0906: A=1.392
S7031-0907: A=2.928
S7031-0908: A=6.000

KMPDA0048EC

S7031-1006/-1007/-1008



S7031-1006: B=1.392
S7031-1007: B=2.928
S7031-1008: B=6.000

KMPDA0049EC

■ Pin connections

Pin No.	S7030 series		S7031 series		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	$R_L=10\text{ k to }100\text{ k}\Omega$
3	OD	Output transistor drain	OD	Output transistor drain	+20 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same pulse as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	0 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	0 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG *20	Transfer gate	TG *20	Transfer gate	Same pulse as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Connect to RD
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	0 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	0 V
24	RG	Reset gate	RG	Reset gate	

*20: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

■ Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S7031-0906/-0907/-0908	S7031-1006/-1007/-1008	Unit
Internal resistance	Rint	Ta=25 °C	2.5	1.2	Ω
Maximum current *21	I _{max}	T _c *22=Th *23=25 °C	1.5	3.0	A
Maximum voltage	V _{max}	T _c *22=Th *23=25 °C	3.8	3.6	V
Maximum heat absorption *24	Q _{max}		3.4	5.1	W
Maximum temperature of heat radiating side	-		70	70	°C

*21: Maximum current I_{max}:

If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.

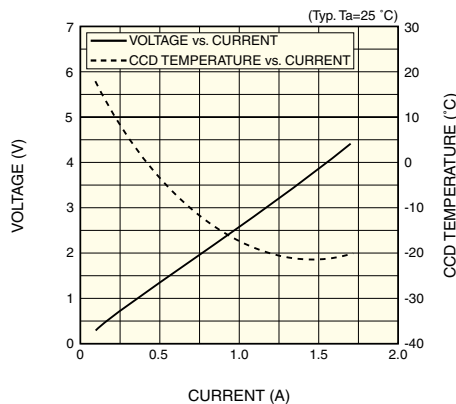
*22: Temperature of the cooling side of thermoelectric cooler.

*23: Temperature of the heat radiating side of thermoelectric cooler.

*24: Maximum heat absorption Q_{max}.

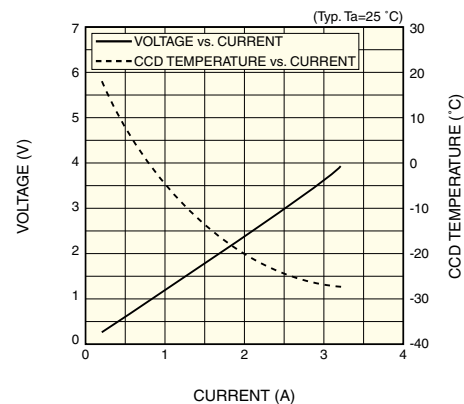
This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.

S7031-0906/-0907/-0908



KMPDB0178EA

S7031-1006/-1007/-1008



KMPDB0179EA

■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_1 = R_2 \times \exp\left(\frac{1}{T_1} - \frac{1}{T_2}\right) \times B$$

where R1 is the resistance at absolute temperature T1 (K)

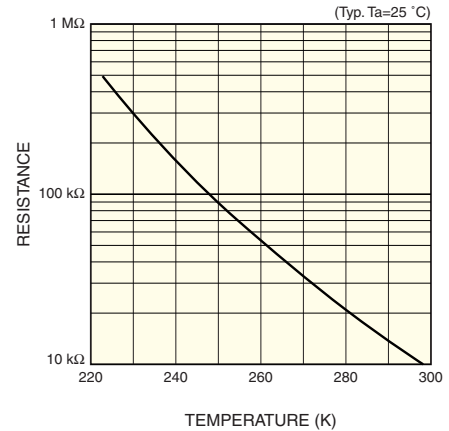
R2 is the resistance at absolute temperature T2 (K)

B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.

$$R(298K) = 10 \text{ k}\Omega$$

$$B(298K / 323K) = 3450 \text{ K}$$



KMPD80111EA

■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

Multichannel detector heads C7040, C7041

Features

- C7040: for S7030 series
C7041: for S7031 series
- Area scanning or full line-binning operation
- Readout frequency: 250 kHz
- Readout noise: 20 e⁻rms
- ΔT=50 °C (ΔT changes by cooling method.)

Input	Symbol	Value
Supply voltage	VD1	+5 Vdc, 200 mA
	VA1+	+15 Vdc, +100 mA
	VA1-	-15 Vdc, -100 mA
	VA2	+24 Vdc, 30 mA
	VD2	+5 Vdc, 30 mA (C7041)
	Vp	+5 Vdc, 2.5 A (C7041)
	VF	+12 Vdc, 100 mA (C7041)
Master start	φms	HCMOS logic compatible
Master clock	φmc	HCMOS logic compatible, 1 MHz



HAMAMATSU

Information furnished by HAMAMATSU is believed to be reliable. However, no responsibility is assumed for possible inaccuracies or omissions. Specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein. ©2003 Hamamatsu Photonics K.K.

HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Hamamatsu City, 435-8558 Japan, Telephone: (81) 053-434-3311, Fax: (81) 053-434-5184, <http://www.hamamatsu.com>

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658

France: Hamamatsu Photonics France S.A.R.L.: 8, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741